BYPASS CIRCUITRY FOR USE IN A PIPELINED PROCESSOR

ABSTRACT OF THE DISCLOSURE

There is disclosed a data processor that uses bypass circuitry to transfer result data from late pipeline stages to earlier pipeline stages in an efficient manner and with a minimum amount of wiring. The data processor comprises: 1) an instruction execution pipeline comprising a) a read stage; b) a write stage; and c) a first execution stage comprising E execution units that produce data results from data operands. The data processor also comprises: 2) a register file comprising a plurality of data registers, each of the data registers being read by the read stage of the instruction pipeline via at least one of R read ports of the register file and each of the data registers being written by the write stage of the instruction pipeline via at least one of W write ports of the register file; and 3) bypass circuitry for receiving data results from output channels of source devices in at least one of the write stage and the first execution stage, the bypass circuitry comprising a first plurality of bypass tristate line drivers having input channels coupled to first output channels of a first plurality of source devices and tristate output channels coupled to a first common read data channel in the read stage.